B KRISHNAN IYER

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SUMMARY

Currently, my research focuses on ***in-network computation*** and ***reconfiguration*** support in hardware, specifically FPGAs. This enables users to push on-demand hardware acceleration, offering a superior alternative to limited rigid ASIC acceleration or higher latency on-path CPUs.

My interests lie in the intersection of computer architecture and embedded system design, where I am deeply passionate about understanding different system designs and making contributions that enhance performance and efficiency. I have worked on diverse projects, including the development of various hardware designs for FPGAs, real-time embedded systems for robotics, and the optimization of multimedia decoding algorithms using SIMD architecture. Each of these experiences has contributed to a better and clearer understanding of different compute systems and architectures, enabling me to make informed design decisions. My contributions involved development of flexible interfaces between compute and data while focusing on energy efficiency and minimal silicon footprint. Some of these interfaces include PCIe, USB, I2C, CAN, etc. My experience spans from low-level firmware development to high-level system architecture, supported by proficiency in programming languages such as C, Assembly, Verilog, Go and Python.

EDUCATION

KAUST (King Abdullah University of Science and Technology) Jan 2023 - Dec 2024 (exp.)
M.S. in Computer Science
GPA: 3.79/4.0

Amrita Vishwa Vidyapeetham Apr 2016 - Aug 2020
B.Tech. in Electrical and Electronics Engineering.
GPA: 8.61/10

WORK EXPERIENCE

Space Telelink May 2022 – Jan 2023
Embedded Researcher

- Implemented multiple device enumeration over a single USB controller (Infineon's FX3), i.e., a composite driver. The driver included HID, mass storage, and a FAT32 file management driver with basic file seek, read, and write functions.
- Explored Ethernet over USB protocols, including RNDIS. This required efficient management of different DMA channels in sync with various USB transfers such as control, interrupt, and bulk transfers. The project led to a fast enumeration of USB peripherals with decent bandwidth, enough to support USB 3.0.
- Implemented a scalable CAN-based communication network for a manipulator robot, resulting in a simplified cable harness and reduced power consumption.

Peer Robotics Jun 2020 – May 2022
Embedded Systems Engineer

- Re-designed and optimized sensor integration system for real-time communication. The work reduces number of components and gives room for tuning of the sensor response parameters according to the system requirements. Work impacted in reduction of communication ports, simplifies cabling, scalable to integrate multiple sensors without adding any overhead processing to the system.
- Developed **AVR based power distribution board**'s firmware with custom drivers for all the peripherals. Executed real time operations by synchronizing with timers and interrupts. Scarcity of timers for different routines also led to the development and integration of a leapfrog mechanism, eliminating need for porting RTOS altogether.
- Developed VRU subsystem based on BNO080. The board involved a bridge (USB - I2C) microcontroller (STM32 - Cortex M0) to handle real-time responses and configuration of VRU. Other interfaces were provided for indicator controls.

- Developed **Health Care module** as part of **QDIC (Qualcomm Design in India Challenge)**. The module was built around SC66-E module and dealt with interfacing RFID sensor (over I2C) and IO.
- Developed **Human Robot Interaction** algorithm based on actuator's data enabling user to drive the robot manually by force without actually feeling the weight of the load on the robot and the robot itself.
- Designed and implemented communication and system's architecture for 250 kg payload product which included Siemens PLC, Modbus Protocol, CAN bus. Also, developed various drivers for supporting hardware like OPC UA, CAN, and OpenCAN.
- Designed and developed auto-charging system for the RM100 and RM250 (mobile robots). The project involved interface protocol development over Siemens S7 PLC and state execution in the robot.
- During the development process, I also played a critical role in deploying robots across various warehouses and coordinating with on-ground personnel to ensure effective management.

PROJECTS

OpenNIC Ext. Jul 2023 - Now
Supervisor: Prof. Suhaib Fahmy KAUST

- Extended OpenNIC *(by Xilinx)* to support Partial Reconfiguration, including adding support for storing bitstreams in on-board DDR and on-chip HBM via Ethernet or PCIe.
- The design included interfacing AXI Stream to AXI MM and directing data stream to memory controllers or ICAP.
- Developed an asynchronous FIFO to support Clock Domain Crossing (CDC) of peripherals as part of the design.

ARM NEON Optimisation Feb 2019 – Dec 2019
Google Summer of Code'19 dav1d, VideoLAN

- Achieved significantly faster execution of various functions compared to C implementation by using assembly language with SIMD architecture on ARM Cortex A53 and A73.
- Programmed crucial modules such as blend, inverse transformation matrix, and intra prediction, achieving a performance improvement of 10x(approx.) over the C implementation.
- Utilized optimization techniques including loop unrolling, memory alignment, and instr. reordering.
- The project resulted in extended runtime for decoding video on apps supporting dav1d on a single charge.

SDHCI MMC Driver May 2018 – Aug 2018
Google Summer of Code'18 Haiku OS

- Implemented support for SDHCI controller according to SD Host controller spec. for Haiku OS on x86 arch.
- Project involved discovering devices on PCI bus and registering child nodes through different bus and device drivers. Controller registers were accessed through MMIO.
- Implemented driver compliant with SD specification 8.0. Finally, read/write functions were implemented in the kernel space. Message Signaled interrupts (MSI) were also implemented in the driver.

Pac-Man (w/ VGA Driver) - *FPGA Game* Oct 2023 – Dec 2023
CS256 - Digital Design KAUST

- Developed Pac-Man to run on an Artix-based FPGA. The project involved creating a VGA driver, collision control, memory management, and game logic. Additionally, GPIOs along with push buttons were used to control the protagonist.
- Implemented a memory interface for users to upload a custom world map and score counter. The world map logic efficiently scaled the map while minimizing memory footprint.

RISC Processor Oct 2023 – Dec 2023
CS258 - Computer Architecture KAUST

- Implemented a simple 64-bit, 5-stage pipelined *scalar* RISC processor. The processor supported double-precision data formats and basic arithmetic operations.
- Demonstrated basic cases for data, structural and control hazards.
- Developed automation scripts for rigorous testing and created test benches for the processor.

PUBLICATIONS

[1] S. Fahmy and K. Iyer, "Dynamic and partial reconfiguration of fpgas," in *Handbook of Computer Architecture*, A. Chattopadhyay, Ed. Singapore: Springer Nature Singapore, 2024.

VOLUNTEERING

- **VDD '19** – Developer – Speaker at VideoLAN Dev Days, '19 Tokyo and presented optimization techniques over SIMD on ARM architecture. Dec 2019
- **FOSS@Amrita** – Mentor, amFOSS - amFOSS is India's Leading Free and Open-source club. My role involved mentoring several team members and students. During this period, I have also organized and took multiple training sessions for college students. Jun 2018 - Apr 2020

SKILLS/HOBBIES

Programming Languages	C, Assembly, Verilog, Go, C++, Python
Tools & Platforms	ARMv8-A&7, PIC micr., AVR micr., Matlab, Siemens PLCs, Xilinx FPGAs, ROS, Infineon's EZ-USB FX3, Proteus